Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A digital signal processor comprising:

a programmable, multiply and accumulate mathematical processor;

an input processor [[that]] to process ~~processes~~ input signals ~~to the digital signal processor~~ received from a receive buffer coupled to said input processor;

an output processor [[that]] to process ~~processes~~ output signals ~~from the digital signal processor~~ to be output via a transmit buffer coupled to said output processor;

a master processor ~~that controls~~ to control said mathematical processor, said input processor and said output processor, and to provide ~~provides the~~ timing for the other processors; and

a storage to store data from each of said processors so as to be ~~selectively~~ accessible by each of said processors, said storage including a plurality of registers, including a first register to transfer existing data from said first register to a second register when new data is written into said first register

~~wherein each of said processors has a different instruction set than the other processors~~.

Claim 2 (currently amended): The digital signal processor of claim 1 further including a random access memory processor ~~that stores~~ to store intermediate calculation results.

Claim 3 (original): The digital signal processor of claim 2 including a bus coupling each of said processors to said storage.

Claim 4 (original): The digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations.

Claim 5 (canceled)

Claim 6 (currently amended): The digital signal processor of claim 1 wherein said processors are to communicate with one another through said storage.

Claim 7 (currently amended): The digital signal processor of claim 1 wherein each of said processors to use very long instruction words.

Claim 8 (canceled)

Claim 9 (currently amended): The digital signal processor of claim 1 wherein said master processor is to wait [[waits]] for the input processor to complete a given operation.

Claim 10 (original): The digital signal processor of claim 1 wherein each of said processors includes its own random access memory.

Claim 11 (canceled)

Claim 12 (currently amended): The digital signal processor of claim [[11]] 1 wherein said input processor is to cause ~~causes~~ the automatic transfer of data.

Claim 13 (currently amended): The digital signal processor of claim [[11]] 1 wherein said mathematical processor is to cause ~~causes~~ said data to be transferred from one register to another.

Claim 14 (currently amended): The digital signal processor of claim 1 ~~including a~~ wherein said mathematical processor which is pipelined.

Claim 15 (original): The digital signal process of claim 1 wherein said mathematical processor is a multi-cycled mathematical processor.

Claim 16 (currently amended): A method of digital signal processing comprising:

using a first processor to process input signals ~~to said digital signal processor~~ received from a receive buffer coupled to said first processor;

using a second processor to process output signals ~~from said signal digital signal processor~~ to be output via a transmit buffer coupled to said second processor;

using a third processor for multiply and accumulate operations;

controlling said first, second and third processors using a fourth processor;

~~enabling each of said processors to store data in a storage and to selectively access said data stored in said storage by another one of said processors~~ storing data from one of said processors in a first register, transferring a prior value stored in said first register into a second register, and transferring a prior value stored in said second register into a third register, when an end of chain value is greater than a start of chain value;

providing [[the]] timing from said fourth processor for each of the other processors~~; and~~

~~providing each of said processors with a different instruction set than the other processors~~.

Claim 17 (canceled)

Claim 18 (currently amended): The method of claim 16 including automatically transferring [[data]] said prior value from [[a]] said first register ~~in said~~ of a storage to a second register ~~in said~~ of said storage when [[new]] said data is being written into said first register.

Claim 19 (currently amended): The method of claim 18 including automatically transferring said prior value [[data]] in response to action by said first processor.

Claim 20 (currently amended): The method of claim 18 including automatically transferring said prior value [[data]] in response to action by said third processor.

Claim 21 (original): The method of claim 18 including storing a bit which indicates which processor may control said automatic transfer of data from one register to another.

Claim 22 (original): The method of claim 16 including accommodating for timing differences between said processors by operating one of said processor in a pipelined fashion.

Claim 23 (original): The method of claim 16 including accommodating differences in processing cycle time of one of said processors by operating said processor in a multi-cycle mode.

Claim 24 (original): The method of claim 23 including holding off said fourth processor when one of said processors is taking more than a cycle to complete an instruction.

Claims 25-30 (canceled)

Claim 31 (new): The digital signal processor of claim 1 wherein each of said processors has a different instruction set than the other processors.

Claim 32 (new): The digital signal processor of claim 1 wherein said first register is to transfer said existing data and write said new data in a single clock signal, and said second register is to transfer a second existing data to a third register in said single clock cycle.

Claim 33 (new): The digital signal processor of claim 1 wherein said transfer of said existing data is performed without execution of a register to register move instruction.

Claim 34 (new): The method of claim 16 including providing each of said processors with a different instruction set than the other processors.

Claim 35 (new): The method of claim 16 including performing the transferring by each of said registers in a single cycle.

Claim 36 (new): The method of claim 16 including transferring said prior value without execution of a register to register move instruction.